IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 6, line 10 is amended as follows:

Referring now to FIG. 3, there is illustrated another example timing diagram 300 of initiating command and address signals by a controller to an integrated circuit memory device according to the present invention. As shown in FIG. 3, the command signals 320, such as CS#, RAS#, CAS#, and WE# and address signals 330, such as BA0~2 and A12~8 are initiated by the controller during a rising edge 302 of a clock cycle of a CK 310. In addition, the address signals, such as A0~7 are initiated during a falling edge 304 of the clock cycle of the CK 310 to increase the transfer rate of the command and address signals during the clock cycle for a given number of command and address pins in a DRAM device. Again it can be envisioned that using an inverse clock signal (CK#) 312 shown in FIG. 3 and initiating command and address signals as described-above can also increase the transfer rate of the command and address signals 320 and 330 sent by the controller during the clock cycle.